Core.L.1

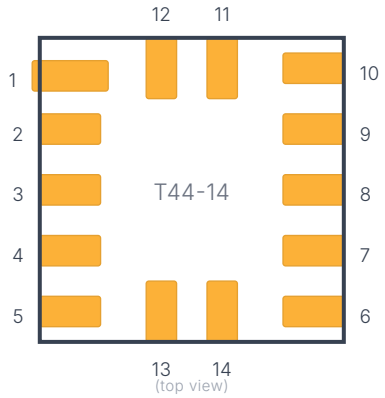
ultra-low-power Cortex-M0+

Ultra-low-power ARM Cortex-M0+ core tile built around the STM32L011E4 with 16KB flash, 2KB RAM, and 512 bytes of data EEPROM. Optimized for battery-powered and energy-harvesting applications, with flexible I/O across 14 pads including I2C, USART, and LPUART interfaces, 6 ADC inputs, multiple timer channels, and dual analog comparators. Runs from 1.8–3.6V with bootloading and hardware debug via SWD.

Overview

Revision	a
Package	T44-14
Supply	1.8–3.6V
Component	STM32L011E4
Interfaces	I2C, USART, LPUART

Pad Assignments



PAD	TYPE	FUNCTION	NOTE
1	power	GND	
2	digital	A3	
	analog	ADC3	
	timer	TIM21.2	
	timer	TIM2.4	
	interface	USART2.RX	
	interface	LPUART1.RX	
	other	COMP2.IN+	
3	digital	A0	
	analog	ADC0	
	timer	TIM2.1	
	timer	TIM2.ETR	
	timer	LPTIM1.1	
	interface	USART2.RX	
	interface	USART2.CRS	
	interface	LPUART1.RX	
	other	COMP1.OUT	
	other	COMP1.IN-	
4	digital	B6	

	interface	I2C1.CLK
	timer	TIM2.3
	timer	LPTIM1.ETR
	interface	USART2.TX
	interface	LPUART1.TX
	other	COMP2.IN+
5	digital	B7
	interface	I2C1.DAT
	timer	TIM2.4
	timer	LPTIM1.2
	interface	USART2.RX
	interface	LPUART1.RX
	other	COMP2.IN+
6	digital	A1
	interface	I2C1.SMBA
	analog	ADC1
	timer	TIM2.2
	timer	TIM21.ETR
	timer	LPTIM1.2
	interface	USART2.RTS_DE
	interface	LPUART1.TX
	other	COMP1.IN+
7	digital	A2
	analog	ADC2
	timer	TIM21.1
	timer	TIM2.3
	interface	USART2.TX
	interface	LPUART1.TX
	other	COMP2.OUT
	other	COMP2.IN-
8	digital	A5
	analog	ADC5
	timer	TIM2.1
	timer	TIM2.ETR
	timer	LPTIM1.2
	other	COMP1.IN-
	other	COMP2.IN-
9	digital	B0
	analog	ADC8
	timer	TIM2.2
	timer	TIM2.3
	interface	USART2.RTS_DE

10	power	V+	1.8-3.6V
11	digital	B9	
	system	BOOT0	
12	system	NRST	
13	digital	A14	
	interface	I2C1.SMBA	
	timer	LPTIM1.OUT	
	interface	USART2.TX	
	interface	LPUART1.TX	
	other	COMP2.OUT	
	system	SWCLK	
14	digital	A13	
	interface	I2C1.DAT	
	timer	LPTIM1.ETR	
	interface	LPUART1.RX	
	other	COMP1.OUT	
	system	SWDIO	

Interfaces

I2C1 I2C

Mode: master, slave

Address: programmable

FUNCTION	REQ	PAD(S)
I2C1.CLK	No	4
I2C1.DAT	No	5, 14
I2C1.SMBA	No	6, 13

USART2 USART

FUNCTION	REQ	PAD(S)
USART2.RX	No	2, 3, 5
USART2.CRS	No	3
USART2.TX	No	4, 7, 13
USART2.RTS_DE	No	6, 9

LPUART1 LPUART

FUNCTION	REQ	PAD(S)
LPUART1.RX	No	2, 3, 5, 14
LPUART1.TX	No	4, 6, 7, 13

Application Notes

Single-Wire Debug & Bootloading

The single-wire debug port is available on pads 13 (SWCLK) and 14 (SWDIO). While not absolutely required, it is often helpful to have the ability to hold pads 22 (NRST) low when connecting to the debugger. You can likely also use BOOT0 to help the debugger connect.

LED

The onboard LED is connected to PA8 in an active-high configuration.