Core.ST.H5.1

250MHz Cortex-M33

The Core.ST.H5.1 is built around the high-performance STM32H523 250-MHz 32-bit Cortex-M33 processor into a single T44 tile, providing a user-configurable combination of multiple communication interfaces (USB 2.0 full-speed, I2C/I3C, SPI, FDCAN, and UART), along with two 12-bit 5-Msps ADC inputs, one DAC output, and multiple timers.

Overview

Revision	a
Package	T44-14
Power	1.71–3.6V (note that a voltage of at least 3.0V is required for USB communications)
Component	STM32H523HE
Interfaces	I2C, SPI, UART, FD CAN, USB, I3C

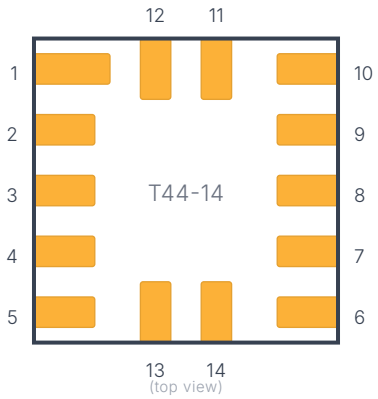
Onboard Features

Status LED	Red · PA15 · (active-high)
Clock	64 MHz HSI · 4 MHz CSI — boots HSI

Configuration

GPIO pad configuration	EXTI · Pull · Speed · Direction · Output default
Pad function assignments	10 pads — see Pad Assignments
Clock configuration	Low (4MHz, CSI) · Medium (64MHz, HSI) (default) · High (128MHz, HSI + PLL) · Max (248MHz, HSI + PLL)
Programming methods	USB DFU · USART1 · USART2 · USART3 · I²C1 · I²C2 · SPI1 · SPI2 · FDCAN1
Interfaces	USB · I²C1 · I²C3 · I3C1 · I3C2 · SPI1 · UART4 · FDCAN1 (enable / role / speed configurable)

Pad Assignments



PAD	TYPE	FUNCTION	NOTE
1	power	GND	
2	digital	A8	
	digital	USB.SOF	
	digital	I2C3.CLK	
	digital	I3C2.CLK	
	digital	SPI1.RDY	
	timer	TIM1.1	
	timer	TIM8.BKIN2	
3	digital	B4	
	digital	I2C3.DAT	
	digital	I3C2.DAT	
	digital	SPI1.MISO	
	timer	TIM3.1	
	timer	LPTIM1.2	
4	digital	B8	
	digital	I2C1.CLK	
	digital	I3C1.CLK	
	timer	TIM4.3	
	digital	UART4.RX	
	digital	FDCAN1.RX	
5	digital	B7	
	digital	I2C1.DAT	
	digital	I3C1.DAT	
	timer	TIM4.2	
	digital	FDCAN1.TX	
6	digital	A12	
	digital	USB.DP	
	timer	TIM1.ETR	
	digital	UART4.TX	
	digital	FDCAN1.TX	
7	digital	A11	
	digital	USB.DM	
	timer	TIM1.4	
	digital	UART4.RX	
	digital	FDCAN1.RX	
8	digital	A7	
	digital	SPI1.MOSI	
	analog	ADC7+	
	analog	ADC3-	
	timer	TIM1.1N	
	timer	TIM3.2	

	timer	TIM8.1N
9	digital	A5
	digital	SPI1.CLK
	analog	ADC19+
	analog	ADC18-
	timer	TIM2.1
	timer	TIM8.1N
	timer	TIM2.ETR
	other	DAC1.OUT
10	power	V+
11	system	BOOT0
12	system	NRST
13	digital	A14
	system	SWCLK
14	digital	A13
	system	SWDIO

Interfaces

I2C1

I2C

Mode: master, slave

Address: programmable

FUNCTION	REQ	PAD(S)
I2C1.CLK	Yes	4
I2C1.DAT	Yes	5

I2C3

I2C

Mode: master, slave

Address: programmable

FUNCTION	REQ	PAD(S)
I2C3.CLK	Yes	2
I2C3.DAT	Yes	3

SPI1

SPI

Mode: master

Max Clock: 45MHz

FUNCTION	REQ	PAD(S)
SPI1.MISO	Yes	3
SPI1.MOSI	Yes	8
SPI1.CLK	Yes	9
SPI1.RDY	No	2

UART4

UART

FUNCTION	REQ	PAD(S)
UART4.RX	No	4, 7
UART4.TX	No	6

FDCAN1

FD CAN

FUNCTION	REQ	PAD(S)
FDCAN1.RX	No	4, 7
FDCAN1.TX	No	5, 6

USB

USB

FUNCTION	REQ	PAD(S)
USB.DP	Yes	6
USB.DM	Yes	7
USB.SOF	No	2

I3C2

I3C

Mode: master, slave

FUNCTION	REQ	PAD(S)
I3C2.CLK	Yes	2
I3C2.DAT	Yes	3

I3C1

I3C

Mode: master, slave

Format: -bit addr

FUNCTION	REQ	PAD(S)
I3C1.CLK	Yes	4
I3C1.DAT	Yes	5

Application Notes

USB 2.0 Full-Speed Port

To utilize the USB 2.0 Full-Speed (12Mbit/s) port, the supply voltage needs to be at least 3.0V. The Core.H.1 can serve as either a peripheral or a host.

USB Bootloading

Similar to the Core.U tiles, when the chip is blank, it will default into the bootloader when connected over USB. Once there is code in the program space, you need to hold the BOOT0 pin low during reset (either power-on or via the NRST pin) to enter the bootloader.

Single-Wire Debug & Bootloading

The single-wire debug port is available on pads 13 (SWCLK) and 14 (SWDIO). While not absolutely required, it is often helpful to have the ability to hold pad 12 (NRST) low when connecting to the debugger. You can likely also use BOOT0 to help the debugger connect.

LED

The onboard LED is connected to PA15 in an active-high configuration.