Core.ST.L0.1

ultra-low-power Cortex-M0+

Ultra-low-power ARM Cortex-M0+ core tile built around the STM32L011E4 with 16KB flash, 2KB RAM, and 512 bytes of data EEPROM. Optimized for battery-powered and energy-harvesting applications, with flexible I/O across 14 pads including I2C, USART, and LPUART interfaces, 6 ADC inputs, multiple timer channels, and an analog comparator. Runs from 1.8–3.6V with bootloading and hardware debug via SWD.

Overview

Revision	a
Package	T44-14
Power	1.8–3.6V
Component	STM32L011E4
Interfaces	I2C, USART, LPUART

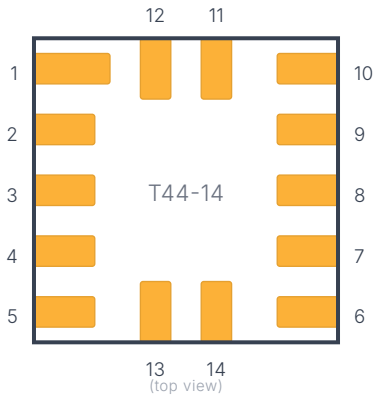
Onboard Features

Status LED	Red · PA8 · (active-high)
Clock	4 MHz MSI · 16 MHz HSI16 — boots MSI

Configuration

GPIO pad configuration	EXTI · Pull · Speed · Direction · Output default
Pad function assignments	11 pads — see Pad Assignments
Clock configuration	Low (1MHz, MSI) · Medium (2MHz, MSI) (default) · High (16MHz, HSI16) · Max (32MHz, HSI16 + PLL)
Programming methods	USART2 · SPI1
Interfaces	I²C1 · USART2 · LPUART1 (enable / role / speed configurable)

Pad Assignments



PAD	TYPE	FUNCTION	NOTE
1	power	GND	
2	digital	A3	
	analog	ADC3	

	timer	TIM21.2
	timer	TIM2.4
	digital	USART2.RX
	digital	LPUART1.RX
3	digital	A0
	analog	ADC0
	timer	TIM2.1
	timer	TIM2.ETR
	timer	LPTIM1.1
	digital	USART2.RX
	digital	USART2.CRS
	digital	LPUART1.RX
	other	COMP1.OUT
	other	COMP1.IN-
4	digital	B6
	digital	I2C1.CLK
	timer	TIM2.3
	timer	LPTIM1.ETR
	digital	USART2.TX
	digital	LPUART1.TX
5	digital	B7
	digital	I2C1.DAT
	timer	TIM2.4
	timer	LPTIM1.2
	digital	USART2.RX
	digital	LPUART1.RX
6	digital	A1
	digital	I2C1.SMBA
	analog	ADC1
	timer	TIM2.2
	timer	TIM21.ETR
	timer	LPTIM1.2
	digital	USART2.RTS_DE
	digital	LPUART1.TX
	other	COMP1.IN+
7	digital	A2
	analog	ADC2
	timer	TIM21.1
	timer	TIM2.3
	digital	USART2.TX
	digital	LPUART1.TX
8	digital	A5

	analog	ADC5	
	timer	TIM2.1	
	timer	TIM2.ETR	
	timer	LPTIM1.2	
	other	COMP1.IN-	
9	digital	B0	
	analog	ADC8	
	timer	TIM2.2	
	timer	TIM2.3	
	digital	USART2.RTS_DE	
10	power	V+	1.8-3.6V
11	digital	B9	
	system	BOOT0	
12	system	NRST	
13	digital	A14	
	digital	I2C1.SMBA	
	timer	LPTIM1.OUT	
	digital	USART2.TX	
	digital	LPUART1.TX	
	system	SWCLK	
14	digital	A13	
	digital	I2C1.DAT	
	timer	LPTIM1.ETR	
	digital	LPUART1.RX	
	other	COMP1.OUT	
	system	SWDIO	

Interfaces

I2C1

I2C

Mode: master, slave

Address: programmable

FUNCTION	REQ	PAD(S)
I2C1.CLK	No	4
I2C1.DAT	No	5, 14
I2C1.SMBA	No	6, 13

USART2

USART

FUNCTION	REQ	PAD(S)
USART2.RX	No	2, 3, 5
USART2.CRS	No	3
USART2.TX	No	4, 7, 13
USART2.RTS_DE	No	6, 9

LPUART1

LPUART

FUNCTION	REQ	PAD(S)
LPUART1.RX	No	2, 3, 5, 14
LPUART1.TX	No	4, 6, 7, 13

Application Notes

Single-Wire Debug & Bootloading

The single-wire debug port is available on pads 13 (SWCLK) and 14 (SWDIO). While not absolutely required, it is often helpful to have the ability to hold pads 22 (NRST) low when connecting to the debugger. You can likely also use BOOT0 to help the debugger connect.

LED

The onboard LED is connected to PA8 in an active-high configuration.