Core.ST.L4.2

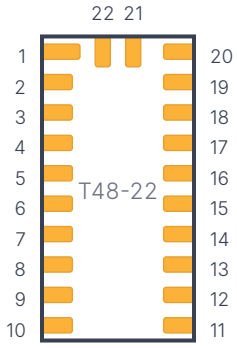
expanded-I/0 USB-prog. Cortex-M4

The expanded-I/O USB-programmable Core.U.2 is based on the same 80-MHz Cortex-M4 STM32L422 as the smaller Core.ST.L4.1, with the top 12 pads (1-5 and 16-22) matching the pad layout of the Core.U.1. The additional I/O pads provide a user-configurable combination of single-wire and trace debugging, two I2C ports, one SPI port, one quad SPI port, ten 12-bit ADC inputs, multiple timers, capacitive-touch inputs, and an on-board comparator. The board also includes an onboard LED and a physical button for reset and bootloading (see Application Notes).

Overview

Revision	a
Package	T48-22
Power	1.8–3.6V (for USB communications, the supply voltage should be greater than 3.0V)
Component	STM32L422TB
Interfaces	I2C, SPI, USB, USART, LPUART, QSPI

Pad Assignments



(top view)

PAD	TYPE	FUNCTION	NOTE
1	power	GND	
2	digital	A7	
	digital	I2C3.CLK	
	digital	SPI1.MOSI	
	analog	ADC12	
	timer	TIM1.1N	
	digital	QSPI.IO2	
3	digital	A1	
	digital	I2C1.SMBA	optional SMBus alert
	digital	SPI1.CLK	
	analog	ADC6	
	timer	TIM2.2	

	timer	TIM15.1N	
	other	COMP1.+	
	digital	USART2.RTS_DE	
4	digital	B6	
	digital	I2C1.CLK	
	timer	TIM16.1N	
	timer	LPTIM1.ETR	external trigger
	digital	USART1.TX	
	other	G2.IO3	
	system	TRACE.D3	
5	digital	B7	
	digital	I2C1.DAT	
	timer	LPTIM1.2	
	digital	USART1.RX	
	system	TRACE.CK	
	other	G2.IO4	
6	digital	A3	
	digital	QSPI.CLK	
	analog	ADC8	
	timer	TIM2.4	
	timer	TIM15.2	
	digital	USART2.RX	
	digital	LPUART1.RX	
7	digital	A2	
	digital	QSPI.CS	
	analog	ADC7	
	timer	TIM2.3	
	timer	TIM15.1	
	digital	USART2.TX	
	digital	LPUART1.TX	
8	digital	A0	
	analog	ADC5	
	timer	TIM2.1	
	timer	TIM2.ETR	
	digital	USART2.CTS	
	other	COMP1.IN-	
	other	COMP1.OUT	
9	digital	A6	
	digital	SPI1.MISO	
	digital	QSPI.IO3	
	analog	ADC11	
	timer	TIM1.BKIN	

	timer	TIM16.1	
	digital	LPUART1.CTS	
	other	COMP1.OUT	
10	digital	A5	
	digital	SPI1.CLK	
	analog	ADC10	
	timer	TIM2.1	
	timer	TIM2.ETR	
	timer	LPTIM2.ETR	
	other	COMP1.IN-	
11	digital	B0	
	system	TRACE.D1	
	digital	SPI1.CS	
	digital	QSPI.IO1	
	analog	ADC15	
	timer	TIM1.2N	
	other	COMP1.OUT	
12	digital	B3	
	system	TRACE.SWO	
	digital	SPI1.CLK	
	timer	TIM2.2	
	digital	USART1.RTS_DE	
13	digital	A14	
	system	SWCLK	
	digital	I2C1.SMBA	
	timer	LPTIM1.OUT	
14	digital	A13	
	system	SWDIO	
15	digital	B1	
	system	TRACE.D1	
	digital	QSPI.IO0	
	analog	ADC16	
	timer	TIM1.3N	
	timer	LPTIM2.1	
	digital	LPUART1.RTS_DE	
16	digital	A12	
	digital	SPI1.MOSI	
	timer	TIM1.ETR	external trigger
	digital	USART1.RTS_DE	RS232 ready-to-send / RS485 driver-enable
	digital	USB.DP	
17	digital	A11	
	digital	SPI1.MISO	

	timer	TIM1.4	
	timer	TIM1.BKIN2	break input to disable PWM output
	timer	TIM1.BKIN2_COMP1	break input to disable PWM output based on COMP1 output
	digital	USART1.CTS	RS232 clear-to-send
	other	COMP1.OUT	
	digital	USB.DM	
	other	G2.IO1	
18	digital	B4	
	digital	I2C3.DAT	
	digital	SPI1.MISO	
	digital	USART1.CTS	RS232 clear-to-send
	other	G2.IO1	
19	digital	A4	
	digital	SPI1.CS	
	timer	LPTIM2.OUT	break input to disable PWM output
	other	COMP1.-	
20	power	V+	1.71-3.6V (>=3.3V for USB)
21	system	BOOT0	internal pull-down defaults to run mode, hold high during reset to enter bootloader (or use the button described in the Application Note section)
	digital	PH3	
22	system	NRST	active-low reset with internal pull-up

Interfaces

I2C1

I2C

Mode	master, slave
Max Clock	1MHz
Address	programmable
Format	7-bit addr

FUNCTION	REQ	PAD(S)
I2C1.CLK	Yes	4
I2C1.DAT	Yes	5
I2C1.SMBA	No	3, 13

I2C3

I2C

Mode	master, slave
Max Clock	1MHz
Address	programmable
Format	7-bit addr

FUNCTION	REQ	PAD(S)
I2C3.CLK	Yes	2
I2C3.DAT	Yes	18

SPI1

SPI

Mode	master, slave
Max Clock	40Mhz (master), 20MHz (slave)

FUNCTION	REQ	PAD(S)
SPI1.CLK	No	3, 10, 12
SPI1.MOSI	No	2, 16
SPI1.MISO	No	9, 17, 18
SPI1.CS	No	11, 19

USB

USB

FUNCTION	REQ	PAD(S)
USB.DP	Yes	16
USB.DM	Yes	17

USART1

USART

FUNCTION	REQ	PAD(S)
USART1.TX	Yes	4
USART1.RX	Yes	5
USART1.RTS_DE	No	12, 16
USART1.CTS	No	17, 18

USART2

USART

FUNCTION	REQ	PAD(S)
USART2.RTS_DE	No	3
USART2.RX	No	6
USART2.TX	No	7
USART2.CTS	No	8

LPUART1 LPUART

FUNCTION	REQ	PAD(S)
LPUART1.RX	No	6
LPUART1.TX	No	7
LPUART1.CTS	No	9
LPUART1.RTS_DE	No	15

QSPI QSPI

FUNCTION	REQ	PAD(S)
QSPI.IO2	Yes	2
QSPI.CLK	Yes	6
QSPI.CS	Yes	7
QSPI.IO3	Yes	9
QSPI.IO1	Yes	11
QSPI.IO0	Yes	15

Application Notes

USB Bootloading

Similar to the Core.U.1, when the chip is blank, it will default into the bootloader when connected over USB. Once there is code in the program space, you need to hold the BOOT0 pin low during reset (either power-on or via the NRST pin) to enter the bootloader. The physical button will also execute this behavior.

Single-Wire Debug & Bootloading

The single-wire debug port is available on pads 13 (SWCLK) and 14 (SWDIO). While not absolutely required, it is often helpful to have the ability to hold pads 22 (NRST) low when connecting to the debugger. You can likely also use BOOT0 (via either the pad or the button) to help the debugger connect.

Button

The board button will issue a software reset via the NRST pin when pressed for a short (less than ~1sec) time. When held for more than ~2 seconds and released, the system will enter the bootloader.

LED

The onboard LED is connected to PA8 in an active-high configuration.