

Core.ST.W5

BLE-enabled 100MHz Cortex M33

The Core.W tile combines the powerful STM32WBA55 100-MHz 32-bit Cortex-M33 processor together with an integrated 2.4GHz antenna on double-size T48 (4.0 x 8.0 mm) SMD package. The tile provides a user-configurable combination of: SW debug & bootloading; 1MB flash & 128KB SRAM; wireless communications (BLE 5.4, Thread, Matter, Zigbee, proprietary); two FM+ (1MHz) I2C ports; two SPI ports; one USART; five 12-bit 2.5Msps ADC inputs (16-bit with oversampling); many timers; ten capacitive touch inputs; one serial-audio interface; IR output; and an on-board LED



Overview	
Revision	b
Package	T48-16
Power	1.8-3.6V
Component	STM32WBA55HGF6
Interfaces	I2C, SPI, USART, SAI

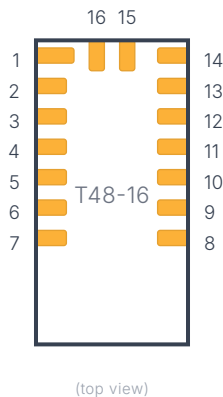
Onboard Features

Status LED	Red · PB12 · (active-high)
Clock	16 MHz HSI16 · 32 MHz HSE — boots HSI16
Integrated 2.4GHz antenna	

Configuration

GPIO pad configuration	EXTI · Pull · Speed · Direction · Output default
Pad function assignments	13 pads — see Pad Assignments
Clock configuration	Low (16MHz, HSI16) · Medium (32MHz, HSE) (default) · High (64MHz, HSE + PLL) · Max (100MHz, HSE + PLL)
Programming methods	USART1 · I ² C3 · SPI3
Interfaces	I ² C1 · I ² C3 · SAI1 · SPI1 · SPI3 · USART2 (enable / role / speed configurable)

Pad Assignments



PAD	TYPE	FUNCTION	NOTE
1	power	GND	
2	digital	A0	



	digital	SPI3.CLK
	analog	ADC9
	timer	TIM1.2N
	timer	TIM3.3
	timer	TIM3.ETR
	timer	LPTIM1.IN1
	other	G2.IO2
3	digital	A5
	digital	SPI3.CS
	analog	ADC4
	timer	TIM2.1
	timer	LPTIM2.ETR
	digital	SAI1.D2
	other	G1.IO4
4	digital	A6
	digital	I2C3.CLK
	analog	ADC3
	timer	TIM2.4
	digital	SAI1.CK2
	digital	SAI1.MCLK_A
	other	G1.IO3
5	digital	A7
	digital	I2C3.DAT
	analog	ADC2
	timer	TIM2.3
	digital	SAI1.SCK_A
	other	G1.IO2
6	digital	B8
	digital	SPI3.MOSI
	timer	TIM1.1
	timer	TIM3.ETR
	timer	TIM16.1N
	timer	LPTIM1.ETR
	digital	USART2.RX
	other	G2.IO4
7	digital	B9
	digital	SPI3.MISO
	analog	ADC10
	timer	TIM1.3N
	timer	TIM3.4
	timer	TIM16.1
	timer	LPTIM2.IN1



	other	G2.IO3	
	digital	IR_OUT	
8	digital	A12	
	digital	SPI1.CS	
	timer	TIM1.2	
	digital	USART2.TX	
	other	G3.IO4	
9	digital	B4	
	digital	SPI1.CLK	
	timer	TIM1.3	
	timer	TIM17.1	
	timer	LPTIM2.IN2	
	digital	USART2.RX	
	digital	SAI1.MCLK_B	
	other	G3.IO1	
10	digital	A15	
	digital	I2C1.CLK	
	digital	SPI1.MOSI	
	timer	TIM1.ETR	
	timer	LPTIM1.2	
	digital	USART2.RTS_DE	
	timer	TIM17.BKIN	
11	digital	B3	
	digital	I2C1.DAT	
	digital	SPI1.MISO	
	timer	TIM1.4	
	timer	TIM17.1N	
	timer	LPTIM1.IN2	
	digital	USART2.CK	
	other	G3.IO2	
12	digital	A13	
	system	SWDIO	
	timer	TIM17.BKIN	
	other	G3.IO3	
13	digital	A14	
	system	SWCLK	
	digital	USART2.TX	
14	power	V+	1.6-3.6V
15	system	BOOT0	
	digital	H3	
16	system	NRST	



Interfaces

I2C1		I2C
Mode	master, slave	
Max Clock	1MHz	
Address	programmable	
FUNCTION	REQ	PAD(S)
I2C1.CLK	Yes	10
I2C1.DAT	Yes	11

I2C3		I2C
Mode	master, slave	
Max Clock	1MHz	
Address	programmable	
FUNCTION	REQ	PAD(S)
I2C3.CLK	Yes	4
I2C3.DAT	Yes	5

SPI1		SPI
Mode	master, slave	
FUNCTION	REQ	PAD(S)
SPI1.CS	No	8
SPI1.CLK	No	9
SPI1.MOSI	No	10
SPI1.MISO	No	11

SPI3		SPI
Mode	master, slave	
FUNCTION	REQ	PAD(S)
SPI3.CLK	No	2
SPI3.CS	No	3
SPI3.MOSI	No	6
SPI3.MISO	No	7

USART2		USART
FUNCTION	REQ	PAD(S)
USART2.RX	No	6, 9
USART2.TX	No	8, 13
USART2.RTS_DE	No	10
USART2.CK	No	11

SAI1		SAI
FUNCTION	REQ	PAD(S)
SAI1.D2	No	3
SAI1.CK2	No	4
SAI1.MCLK_A	No	4
SAI1.SCK_A	No	5
SAI1.MCLK_B	No	9

Application Notes

Single-Wire Debug & Bootloading

The single-wire debug port is available on pads 13 (SWCLK) and 14 (SWDIO). While not absolutely required, it is often helpful to have the ability to hold pads 22 (NRST) low when connecting to the debugger. You can likely also use BOOT0 to help the debugger connect.

Antenna Clearance

For the best wireless performance, the antenna-end of the Tile (the end without any pads) should not have any copper traces or planes above or below it.



LED

The onboard LED is connected to PB12 in an active-high configuration.